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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	042390.P3495C2
First Inventor or Application Identifier	Michael Barrow
Title	PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A
Express Mail Label No.	EL236786933US

jc600 U.S. PTO 03/22/99

jc549 U.S. PTO 09/274430 03/22/99

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

6. ☒ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification [*Total Pages* 14]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (*if filed*)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. ☒ Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 1]

4. Oath or Declaration [*Total Pages* 1]
a. ☐ Newly executed (original copy)
b. ☐ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ☐ Computer Readable Copy
b. ☐ Paper Copy (identical to computer copy)
c. ☐ Statement verifying identity of above copies

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ACCOMPANYING APPLICATION PARTS

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
9. ☐ English Translation Document *(if applicable)*
10. ☐ Information Disclosure Statement (IDS)/PTO - 1449 ☐ Copies of IDS Citations
11. ☐ Preliminary Amendment
12. ☐ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. ☐ *Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired
14. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. ☐ Other: . . . . . .

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 08/959,546

Prior application Information: Examiner D. Foster *Group/Art Unit:* 2835

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

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Our Ref. No.: 042390.P3495C2
Express Mail No. EL236786933US

UNITED STATES PATENT APPLICATION

FOR

PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A POPULATED CENTER

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PREPARED BY:

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BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an integrated circuit package.

2. DESCRIPTION OF RELATED ART

Integrated circuits are typically mounted to a package that is soldered to a printed circuit board. One such type of integrated circuit package is a ball grid array ("BGA") package. BGA packages have a plurality of solder balls located on a bottom external surface of a package substrate. The solder balls are reflowed to attach the package to the printed circuit board. The integrated circuit is mounted to a top surface of the package substrate, and electrically coupled to the solder balls by internal routing within the package.

Figure 1 shows a solder ball array of a prior art BGA package 2. The solder balls 4 are arranged in a two-dimensional pattern across the bottom surface of the package. The integrated circuit 6 is centrally located on the opposite side of the package 2. The package 2 is typically constructed from a material which has a coefficient of thermal expansion that is different than the thermal expansion coefficient of the integrated circuit. It

has been found that the differential thermal expansion between the integrated circuit and the package will induce temperature related stresses that fail solder joints in an area which corresponds to the outer edges of the circuit die.

Figure 2 shows a BGA package 2 of the prior art which has an outer two dimensional array of solder balls 4. The solder balls 4 are located away from the package area that is beneath the integrated circuit 6. Locating the solder balls 4 away from the integrated circuit 6 reduces the thermal stresses on the solder joints created by the differential expansion between the package and the integrated circuit. Although effective in reducing solder failure the outer array pattern limits the input/output (I/O) of the package. Additionally, the integrated circuit generates heat which conducts through the solder balls and into the printed circuit board. Locating the solder balls at the outer perimeter of the package increases the thermal path through the package substrate. The longer path increases the thermal impedance of the package and the junction temperature of the integrated circuit. It would be desirable provide a BGA package that has a longer product life, lower thermal impedance and higher I/O than BGA packages of the prior art.

SUMMARY OF THE INVENTION

The present invention is a ball grid array ("BGA") integrated circuit package which has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls located on a bottom surface of a package substrate. The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted to an opposite surface of the substrate is an integrated circuit that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls are located outside the dimensional profile of the integrated circuit to reduce solder stresses induced by the differential thermal expansion between the integrated circuit and the substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct thermal and electrical path from the integrated circuit to the printed circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects and advantages of the present invention will become more readily apparent to those ordinarily skilled in the art after reviewing the following detailed description and accompanying drawings, wherein:

Figure 1 is a bottom view of a ball grid array integrated circuit package of the prior art;

Figure 2 is a bottom view of a ball grid array integrated circuit package of the prior art;

Figure 3 is a side cross-sectional view of a ball grid array package of the present invention;

Figure 4 is a bottom view of the package shown in Fig. 3;

Figure 5 is a bottom view of an alternate ball grid array package.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 3 and 4 shows a ball grid array ("BGA") integrated circuit package 10 of the present invention. The package 10 includes a substrate 12 that has a top surface 14 and an opposite bottom surface 16. Mounted to the top surface 14 of the substrate 12 is an integrated circuit 16. The integrated circuit 18 is typically a microprocessor. Although a microprocessor is described, it is to be understood that the package 10 may contain any electrical device(s).

The top surface 14 of the substrate 12 has a plurality of bond pads 20 and a ground bus 22. The substrate 12 may also have a separate power bus 23 concentrically located about the integrated circuit 18 and ground pad 22. The integrated circuit 18 is coupled to the bond pads 20 and busses 22 and 23 by bond wires 24. The integrated circuit 16 is typically enclosed by an encapsulant 26. Although bond wires 24 are shown and described, the integrated circuit 18 can be mounted and coupled to the substrate with solder balls located on the bottom surface of the circuit die in a package and process commonly referred to as "C4" or "flip chip" packaging.

The bottom surface 16 of the substrate 12 has a plurality of contact pads 28. The contact pads 28 are coupled to the bond pads 20 and busses 22 and 23 by vias 30

and internal routing 32 within the substrate 12. The substrate can be constructed with conventional printed circuit board, or co-fired ceramic, packaging processes known in the art.

A plurality of solder balls 34 are attached to the contact pads 28 with known ball grid array processes. The solder balls 34 are typically reflowed to attach the package 10 to a printed circuit board (not shown).

The contact pads 28 are arranged in an outer two-dimensional array 36 and a center two-dimensional array 38. Each array contains a plurality of contact pads 28 that are separated from each other by a number of dielectric spaces 40. The outer array 36 is separated from the center array 38 by a dielectric area 42. The outer array 38 is preferably located outside of the outer dimensional profile of the integrated circuit 18. In this manner the solder joints of the outer array 38 are not subjected to stresses created by the difference in the coefficient of thermal expansion of the integrated circuit 18 and the expansion coefficient of the substrate 12. The center array 38 is located near the origin of the integrated circuit 16 in an area that does not undergo as much thermal expansion as the outer edges of the circuit die. Therefore the solder stresses created by the differential thermal expansion is minimal in the area of the center array 38. The separated arrays provide a pattern that minimizes the stresses on the solder joints.

The outer array 36 is typically coupled to the signal lines of the integrated circuit 16. The center array 38 is preferably coupled to the ground bus 20 and power bus 23 of the substrate 12. The vias 30 that couple the busses 22 and 23 to the center contact pads 38 provide a direct thermal path through the substrate. The direct path lowers the thermal impedance of the package 10 and the junction temperature of the integrated circuit 18. Additionally, the short electrical path lowers the self-inductance and reduces the switching noise of the integrated circuit 18.

In the preferred embodiment, the package 10 contains 292 contact pads 28 on a 27 by 27 millimeter (mm) wide substrate 12, or 352 contact pads 28 on a 35 by 35 mm substrate 12. The dielectric space 40 between the contact pads 28 is typically 1.27 mm. The package 10 typically has a height of approximately 2.5 mm.

The package 10 is assembled by attaching the solder balls 34 to the contact pads 28. The integrated circuit 18 is mounted and coupled to the substrate 12. The integrated circuit 18 is then enclosed by the encapsulant 26. The BGA package 10 is typically shipped to an end user that mounts the package 10 to a printed circuit board by reflowing the solder balls 34.

Figure 5 shows an alternate embodiment of a package 10' which has five or six rows of contact pads 28 in the outer array 36' of the substrate 12'. The additional pads 28 increase the input/output (I/O) of the package 10. The

outer array 36' is preferably outside the outer dimensional profile of the integrated circuit 18 to minimize the stresses on the solder joints. The package 10' may provide 324 contact pads 28 on a 27 by 27 mm substrate 10. The longer rows of the package 60 provide the approximate I/O of a 35 by 35 mm package, within the footprint of a 27 by 27 mm package.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.

What is claimed is:

1. A ball grid array package, comprising:

a substrate which has a top surface and an opposite bottom surface, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances; and,

a plurality of solder balls attached to said contact pads of said substrate.

2. The package as recited in claim 1, wherein said top surface of said substrate has a plurality of bond pads.

3. The package as recited in claim 2, wherein said top surface of said substrate has a ground bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

4. The package as recited in claim 3, wherein said outer array of contact pads has at least five rows of contact pads.

5. The package as recited in claim 4, wherein said top surface of said substrate has a power bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

6. The package as recited in claim 5, wherein said center array of contact pads is arranged in a four by four matrix.

7. A ball grid array integrated circuit package, comprising:

a substrate which has a top surface and an opposite bottom surface, said top surface having a plurality of bond pads, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances;

a plurality of solder balls attached to said contact pads of said substrate; and,

an integrated circuit that is mounted to said substrate and coupled to said bond pads.

8. The package as recited in claim 7, wherein said top surface of said substrate has a ground bus that is coupled to said integrated circuit and connected to said center array of contact pads by a plurality of vias that extend through said substrate.

9. The package as recited in claim 8, wherein said outer array of contact pads has at least five rows of contact pads.

10. The package as recited in claim 9, wherein said top surface of said substrate has a power bus that is connected to said center array of contact pads by a plurality of vias that extend through said substrate.

11. The package as recited in claim 10, wherein said center array of contact pads is arranged in a four by four matrix.

12. The package as recited in claim 11, wherein said integrated circuit is enclosed by an encapsulant.

13. The package as recited in claim 7, wherein said outer array of contact pads is located outside an outer dimensional profile of said integrated circuit.

14. A method for assembling a ball grid array integrated circuit package, comprising the steps of:

a) providing a substrate which has a top surface and an opposite bottom surface, said bottom surface having an outer array of contact pads each separated from each other by a first distance, and a center array of contact pads each separated from each other by a second distance, said center array of contact pads being separated from said outer array of contact pads by a third distance which is larger than the first and second distances;

b) mounting an integrated circuit to said top surface of said substrate; and,

c) attaching a plurality of said solder balls to said contact pads.

15. The method as recited in claim 14, further comprising the step of encapsulating said integrated circuit.

16. The method as recited in claim 15, further comprising the step of coupling said integrated circuit to said substrate with a plurality of bond wires.

ABSTRACT OF THE DISCLOSURE

A ball grid array (BGA) integrated circuit package which has an outer two-dimensional array of solder balls and a center two-dimensional array of solder balls located on a bottom surface of a package substrate. The solder balls are typically reflowed to mount the package to a printed circuit board. Mounted to an opposite surface of the substrate is an integrated circuit that is electrically coupled to the solder balls by internal routing within the package. The outer array of solder balls are located the dimensional profile of the integrated circuit to reduce solder stresses induced by the differential thermal expansion between the integrated circuit and the substrate. The center solder balls are typically routed directly to ground and power pads of the package to provide a direct thermal and electrical path from the integrated circuit to the printed circuit board.

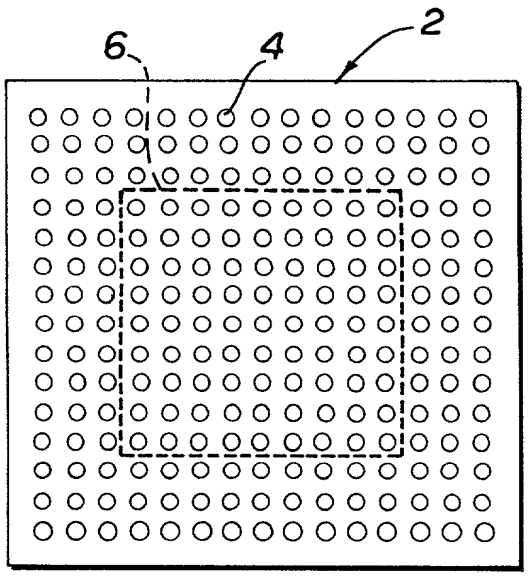

FIG. 1 PRIOR ART

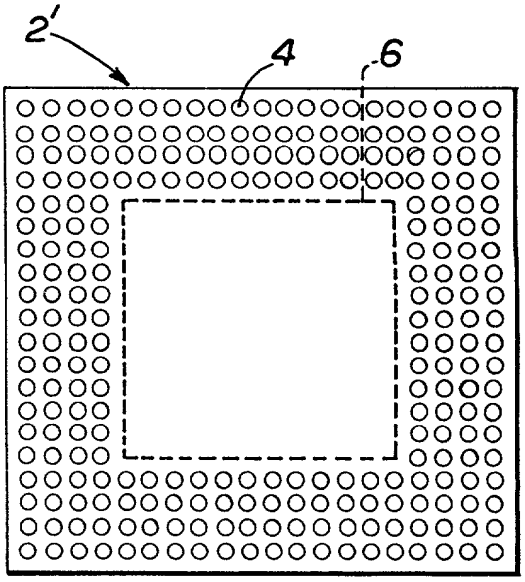

FIG. 2 PRIOR ART

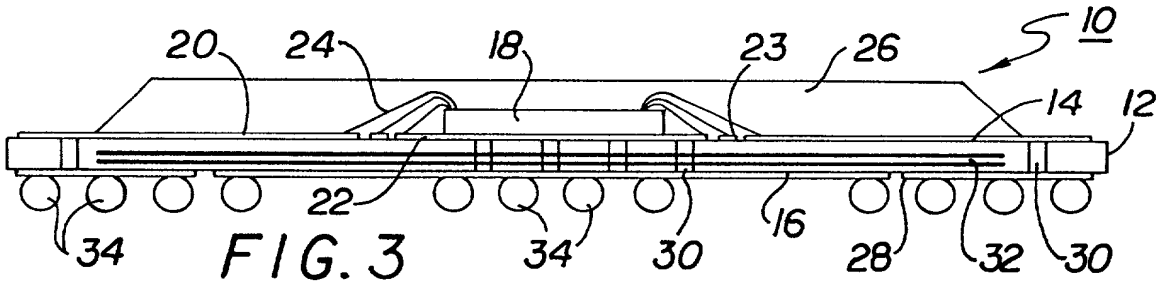

FIG. 3

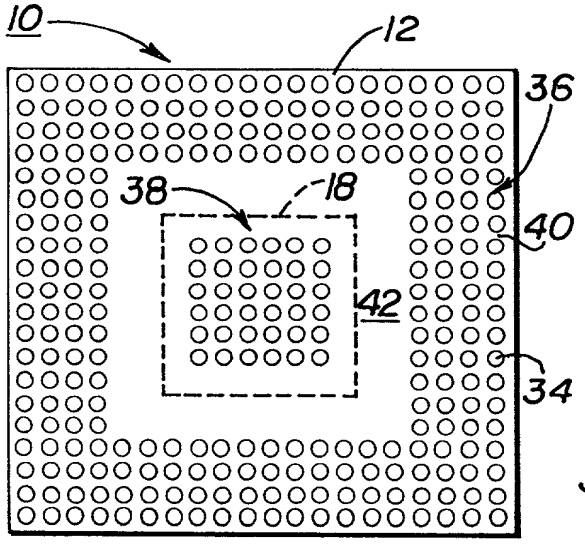

FIG. 4

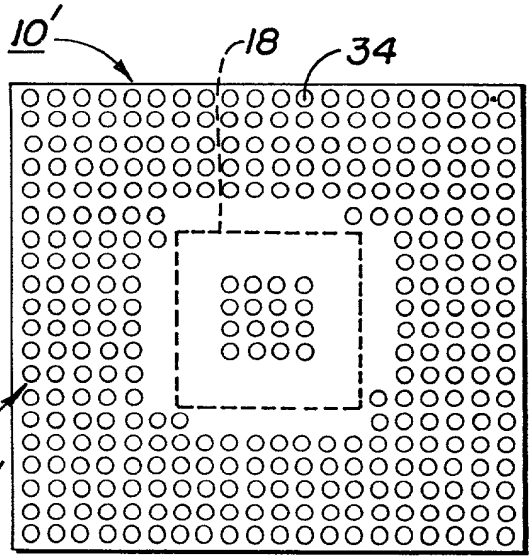

FIG. 5

Our Ref.: 42390.P3495

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

PERIMETER MATRIX BALL GRID ARRAY CIRCUIT PACKAGE WITH A POPULATED CENTER

the specification of which

__XX__ is attached hereto.
_____ was filed on _____ as
Application Serial No. _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I do not know and do not believe that the same was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119, of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status -- patented, pending, abandoned)